REMARKS

Applicant thanks the Examiner for the helpful personal interview which was conducted on May 7, 2002. Applicant notes that at the interview the Examiner recommended amendments to the claims which would help to allow the case. Applicant notes that the recommended claim amendments are made by this Supplemental Amendment. Therefore, Applicant respectfully submits that all of the claims are allowable.

Claims 5-9 and 12-22 are all the claims presently being examined in the application. Claims 5, 12 and 15 have been amended to more particularly define the invention. Attached hereto is a marked-up version of the changes made to the specification and claims by the current Amendment.

It is noted that the claim amendments are made only for more particularly pointing out the invention, and <u>not</u> for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability.

Claims 5 and 12 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Lin (U.S. Pat. 6,107,154). Claims 6-8, 13 and 14 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Lin. Claim 9 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Lin and further in view of Horita et al. (U.S. Pat. 6,303,432).

These rejections are respectfully traversed in view of the following discussion.

I. THE CLAIMED INVENTION

The claimed invention is directed to a method of manufacturing a semiconductor device having a memory cell section and an adjacent circuit section. The method includes forming a metal film directly on surfaces of source-drain regions and gate regions in the memory cell section and the adjacent circuit section, and annealing the device to react the metal film with the surfaces <u>to concurrently form a metal silicide layer in each of the memory cell section and the adjacent circuit section</u>.

Conventional methods typically form a silicide layer in a memory cell portion separately from a silicide layer in a logic portion on a chip. Further, the source-drain regions in the memory cell portion typically have a low dopant concentration, in order to suppress a short channel effect. Therefore, formation of a silicide layer on these source-drain regions causes an increased leakage current.

The claimed method, on the other hand, forms the metal film directly on the surface of source-drain regions and gate regions, and reacts the metal film with surface to concurrently form a metal silicide layer in each of the memory cell and adjacent circuit sections. The source-drain regions may, therefore, be formed with a high dopant concentration, and a leakage current may be substantially eliminated.

II. THE 35 USC §112, SECOND PARAGRAPH REJECTION

The Examiner alleges that claims 5-9 and 12-14 are indefinite for failing to particularly point out and distinctly claim the invention. Specifically, the Examiner alleges that claims 5 and 12 require a salicidation be performed in one step.

Applicant notes, however, that claim 12 (and similarly in claim 5) recites "forming a metal film" and "annealing said device... to form a metal silicide layer".

In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

III. THE PRIOR ART REFERENCES

A. The Lin Reference

The Examiner alleges that Lin teaches the claimed invention. Applicant submits, however, that there are elements of the claimed invention which are neither taught nor suggested by Lin.

Lin discloses a method of fabricating an embedded DRAM device. In the Lin method, the titanium silicide layers in the embedded DRAM device are formed by first performing an SEG (selective epitaxial growth) process so as to form a plurality of amorphous silicon layers over the polysilicon gates and the amorphous silicon layers over the polysilicon gates and the source/drain regions of the various FET (field effect transistor) elements in the embedded DRAM device, and then performing a self-aligning silicide process on these amorphous silicon layers. This allows the titanium silicide layers to be isolated by the source/drain regions from the substrate. Formation of the titanium silicide layers allegedly does not deplete part of the silicon atoms in the substrate as in the prior art, thus allegedly preventing a further thinning of the shallow junction that would cause leakage current in the DRAM device (Lin at Abstract).

However, Lin does not teach or suggest "forming a metal film directly on surfaces of source-drain regions and gate regions in said memory cell section and said adjacent circuit section" nor "annealing said device to react said metal film with said surfaces to concurrently form a metal silicide layer in each of said memory cell section and said adjacent circuit section" both of which are recited in claims 12 and 15, and similarly in claim 5. As explained in the Application, conventional methods typically form a silicide layer in a memory cell portion separately from a silicide layer in a logic portion on a chip (Application at page 4, lines 15-18). Further, the source-drain regions in the memory cell portion typically have a low dopant concentration, in order to suppress a short channel effect. Therefore, formation of a silicide layer on these source-drain regions causes an increased leakage current (Application at page 2, lines 8-15).

The claimed method, on the other hand, forms the metal film directly on the surface of source-drain regions and gate regions, and reacts the metal film with surface to form a metal silicide (Application at Figure 6; page 10, lines 15-21). The source-drain regions may, therefore, be formed with a high dopant concentration, and a leakage current may be substantially eliminated (Application at page 12, line 18-page 13, line 14).

Specifically, it is explained that "[w]hat distinguishes the present invention from the conventional techniques the most is the fact that, even in the memory cell region of the DRAM section, there are formed the S/D regions with a high dopant concentration defined as n^+. When silicide is formed on the S/D regions with such a high dopant concentration, good ohmic contacts can be formed. Further, because the junction becomes deeper, the junction leakage current is hardly generated even if silicide is formed over all the surfaces of the S/D regions. In contrast with this, when silicide is formed on conventional low dopant-concentration regions (n^-), Schottkey contacts are formed therebetween, which is not adequate for the purpose of achieving lower resistance (Application at page 12, line 18-page 13, line 6).

Clearly, Lin does not teach or suggest these novel features. Indeed, as noted above, Lin specifically teaches performing an SEG (selective epitaxial growth) process so as to form a plurality of amorphous silicon layers over the polysilicon gates and the amorphous silicon layers over the polysilicon gates and the source/drain regions of the various FET (field effect transistor) elements in the embedded DRAM device, and then performing a self-aligning

silicide process on these amorphous silicon layers.

In other words, Lin does not form a metal film directly on the source-drain regions and gate regions as in the claimed invention. Instead, Lin forms the metal film on a layer of amorphous silicon layer. Further, Lin does not react a metal film with the surface of the source-drain regions and gate regions. Instead, Lin reacts the metal film with the amorphous silicon layer.

Indeed, the whole point of Lin is to avoid forming the metal film on the source-drain and gate surfaces, in order to avoid depleting "the silicon atoms in the substrate 300 as in the case in the prior art" (Lin at col. 7, lines 48-50). In other words, Lin specifically teaches away from the claimed method.

In summary, Applicant respectfully submits that the production method of Lin per se is different to that of the present invention. In Lin, source/drain regions are formed as in an ordinary logic device so that good ohmic contact can be achieved. Further, the silicide formation is carried out after selectively forming amorphous silicon on the source/drain regions and on the gate so that the silicide is formed above the surface of the substrate. That is, silicon in the substrate is not consumed and, therefore, the formed silicide does not go under the surface of the substrate.

On the other hand, in the present invention, silicon in the substrate is directly consumed by forming silicide so that the silicide layer goes under the surface of the substrate. That is, in the present invention, not only does the manufacturing process differ from the Lin process, but the device structure differs from the Lin device at least with respect to a position of the silicide. Furthermore, Lin's process is actually complicated and if the device size decreases, process margin rapidly decreases so that miniaturization of device is very difficult. In contrast, the process of the present invention is suitable for miniaturization because the surface of the silicon substrate is directly converted to silicide.

Therefore, Applicant submits that the reference does not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection

B. The Horita Reference

The Examiner alleges that Lin would have been combined with Horita to form the

claimed invention. Applicant submits, however, that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

Horita discloses a method of manufacturing a semiconductor device having a DRAM memory cell and logic cell on a single substrate. In the Horita method, after formation of a polysilicon layer which is to act as gate electrodes, silicon nitride films are formed so as to cover source/drain regions of the DRAM memory cell and to cause other source/drain regions and the polysilicon layer to be exposed. A metal silicide layer is formed on the semiconductor substrate by means of a self-aligned silicide technique (Horita at Abstract).

However, like Lin, Horita does not teach or suggest "forming a metal film directly on surfaces of source-drain regions and gate regions in said memory cell section and said adjacent circuit section" nor "annealing said device to react said metal film with said surfaces to concurrently form a metal silicide layer in each of said memory cell section and said adjacent circuit section" both of which are recited in claims 12 and 15, and similarly in claim 5. As explained above, the claimed method forms the metal film directly on the surface of source-drain regions and gate regions, and reacts the metal film with surface to form a metal silicide (Application at Figure 6; page 10, lines 15-21). The source-drain regions may, therefore, be formed with a high dopant concentration, and a leakage current may be substantially eliminated (Application at page 12, line 18-page 13, line 14).

Clearly, Horita does not teach or suggest these novel features. Indeed, similarly to Lin, Horita teaches forming the metal layer on an intervening layer. Specifically, Horita teaches forming a silicon nitride layer 81 on the source-drain regions as noted above (Horita at Figure 8; col. 10, lines 51-64). In fact, Horita specifically states that "since the surfaces f the source/drain regions 10 and 11 are covered with the silicon nitride film 81, the metal silicide layer 7 is not formed thereon (Horita at col. 10, lines 59-64).

In other words, Horita does not form a metal film directly on the source-drain regions as in the claimed invention. Instead, Horita forms the metal film on a layer of silicon nitride. Further, Horita does not react a metal film with the surface of the source-drain regions. Instead, Horita reacts the metal film with the amorphous silicon layer. Therefore, Horita does not make up for the deficiencies of Lin.

Therefore, Applicant submits that these references would not have been combined and

even if combined, the combination would not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection

IV. FORMAL MATTERS AND CONCLUSION

Applicant notes that the title has been amended to be more descriptive, and that specification has been amended to correct the misspelling of "Schottky".

In view of the foregoing, Applicant submits that claims 5-9 and 12-22, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a <u>telephonic or personal interview</u>.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

Date: 5/30/02

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

The specification was amended as follows:

On page 12, paragraph 3 starting on line 18 was amended as follows:

- - What distinguishes the present invention from the conventional techniques the most is the fact that, even in the memory cell region of the DRAM section, there are formed the S/D regions with a high dopant concentration defined as n^+. When silicide is formed on the S/D regions with such a high dopant concentration, good ohmic contacts can be formed. Further, because the junction becomes deeper, the junction leakage current is hardly generated even if silicide is formed over all the surfaces of the S/D regions. In contrast with this, when silicide is formed on conventional low dopant-concentration regions (n^-), <u>Schottky</u> [Schottkey] contacts are formed therebetween, which is not adequate for the purpose of achieving lower resistance. - -

IN THE CLAIMS:

Please amend the claims to read as follows:

5. (Twice Amended) A method of manufacturing a DRAM-incorporated semiconductor device in which a DRAM section and a logic section are formed on a semiconductor substrate that is isolated into elements, said method comprising:

forming a metal film directly on surfaces of source-drain regions and gate regions in said DRAM section and said logic section; and

heat treating said device to react said metal film with said surfaces to <u>concurrently</u> form a metal silicide layer <u>in each of said DRAM section and said logic section</u>.

12. (Twice Amended) A method of manufacturing a semiconductor device having a memory cell section and an adjacent circuit section, said method comprising:

forming a metal film directly on surfaces of source-drain regions and gate regions in said memory cell section and said adjacent circuit section; and

annealing said device to react said metal film with said surfaces to <u>concurrently</u> form a metal silicide layer <u>in each of said memory cell section and said adjacent circuit section</u>.

15. (Amended) A method of manufacturing a semiconductor device comprising:

forming a metal film on source-drain and gate surfaces in a memory cell section of a substrate, and on source-drain and gate surfaces in an adjacent circuit section of said substrate; and

heat treating said device to react said metal film with silicon in said surfaces to concurrently form a metal silicide layer in each of said memory cell section and said adjacent circuit section.